CLAIMS

What is claimed is:

5 1. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

10 creating at least one conductive winding on the at least one dielectric layer; and

creating a P-well having a major surface parallel to a major surface of the dielectric layer.

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2. The method of claim 1 further consists of:

creating a field oxide having a major surface that is juxtaposed to the major surface of the P-well.

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3. The method of claim 1 further consists of:

creating the at least one dielectric layer to include one layer; and

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creating the at least one conductive winding to include a spiral winding on the one layer.

4. The method of claim 1 further consists of:

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creating the at least one dielectric layer to include a plurality of layers; and

creating the at least conductive winding to include a plurality of single windings one the plurality of layers.

5 5. The method of claim 1 further consists of:

creating the at least one dielectric layer to include a plurality of layers; and

- 10 creating the at least conductive winding to include a plurality of spiral windings one the plurality of layers.
 - 6. The method of claim 1 further consists of:
- 15 creating a substrate having a major surface parallel to the major surface of the at least one dielectric layer.
 - 7. The method of claim 1 further consists of:
- 20 creating a secondary winding magnetically coupled to the conductive winding.
 - 8. The method of claim 1, wherein the at least one conductive winding further consists of:

creating a center tap operably coupled to a reference potential to produce a differential inductor.

9. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

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creating at least one conductive winding on the at least one dielectric layer; and

creating a field oxide layer having a major surface 10 parallel to a major surface of the dielectric layer.

10. The method of claim 9 further consists of:

creating a P-well having a major surface that is juxtaposed to the major surface of the field oxide layer.

11. The method of claim 9 further consists of:

creating a secondary winding magnetically coupled to the conductive winding.

- 12. The method of claim 9, wherein the at least one conductive winding further consists of:
- 25 creating a center tap operably coupled to a reference potential to produce a differential inductor.

13. A method for manufacturing an on-chip inductor consisting of:

creating at least one dielectric layer;

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creating at least one conductive winding on the at least one dielectric layer; and

creating poly silicon layer having a major surface parallel to a major surface of the dielectric layer.

14. The method of claim 13 further consists of:

creating a secondary winding magnetically coupled to the conductive winding.

- 15. The method of claim 13, wherein the at least one conductive winding further consists of:
- 20 creating a center tap operably coupled to a reference potential to produce a differential inductor.